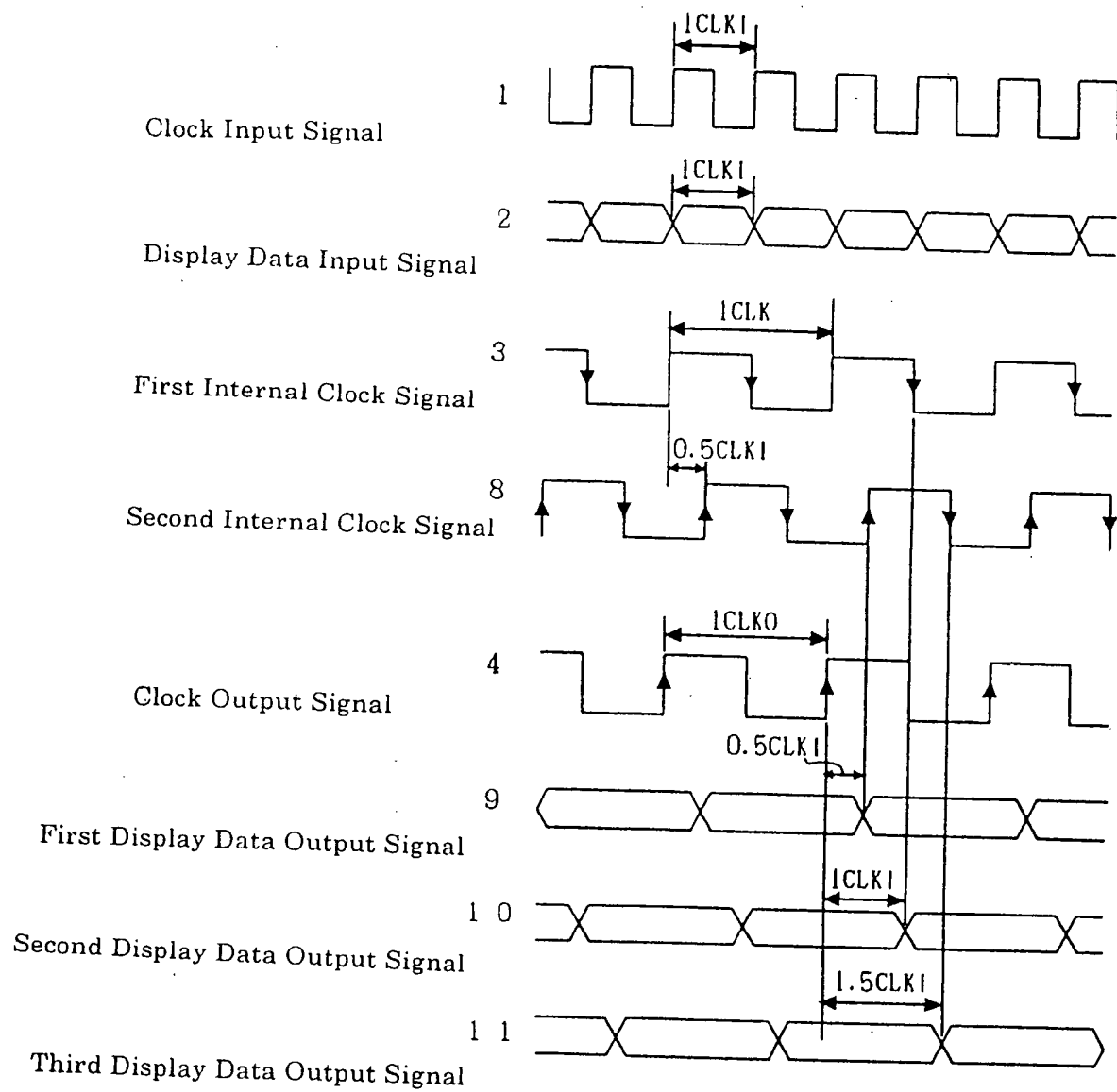




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SN 09/257,506
filed 2/25/99
Matsumura

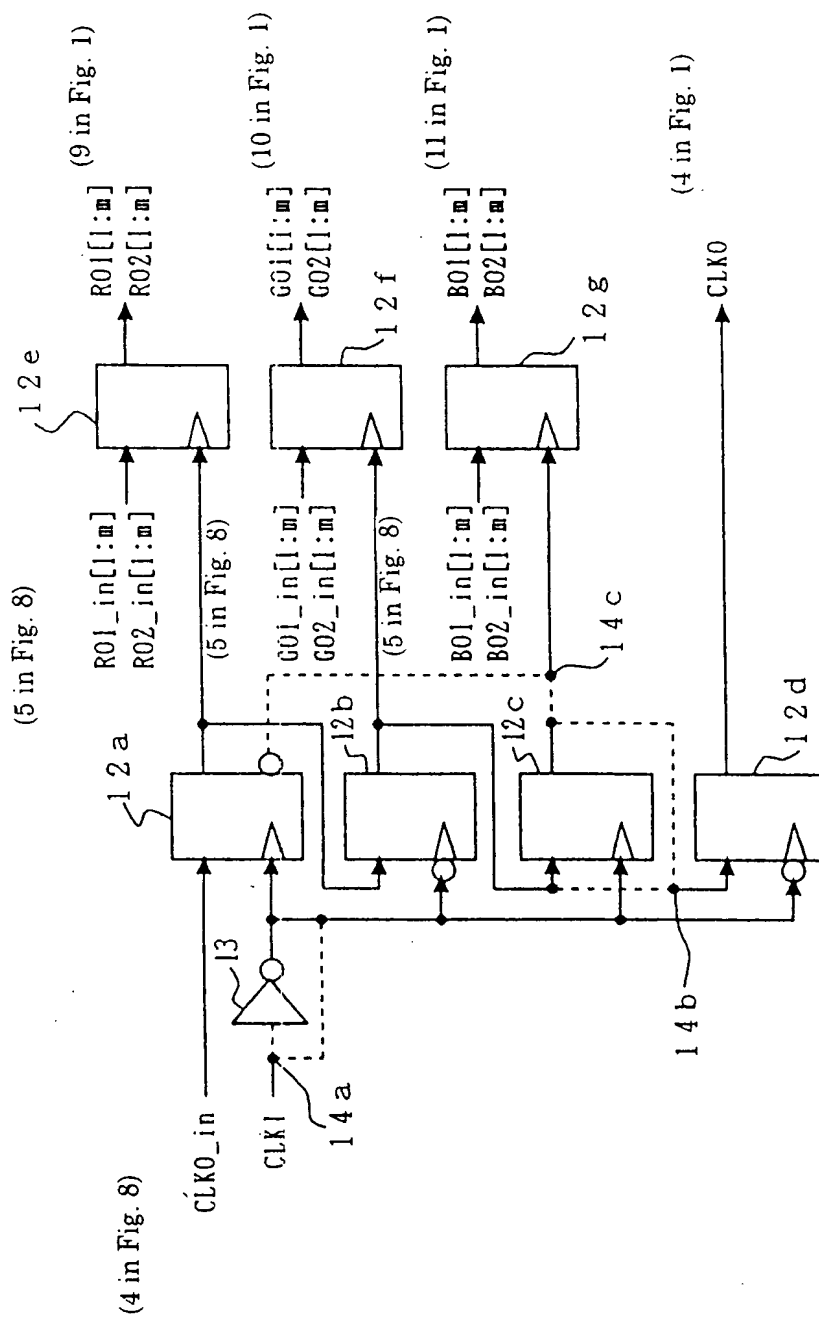
Fig 1





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Fig 2



REPLACEMENT SHEET



Fig 3

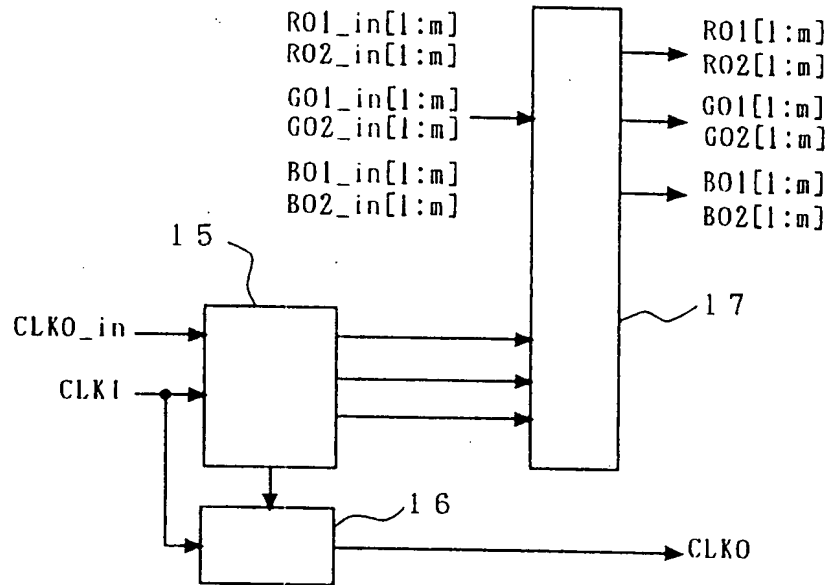
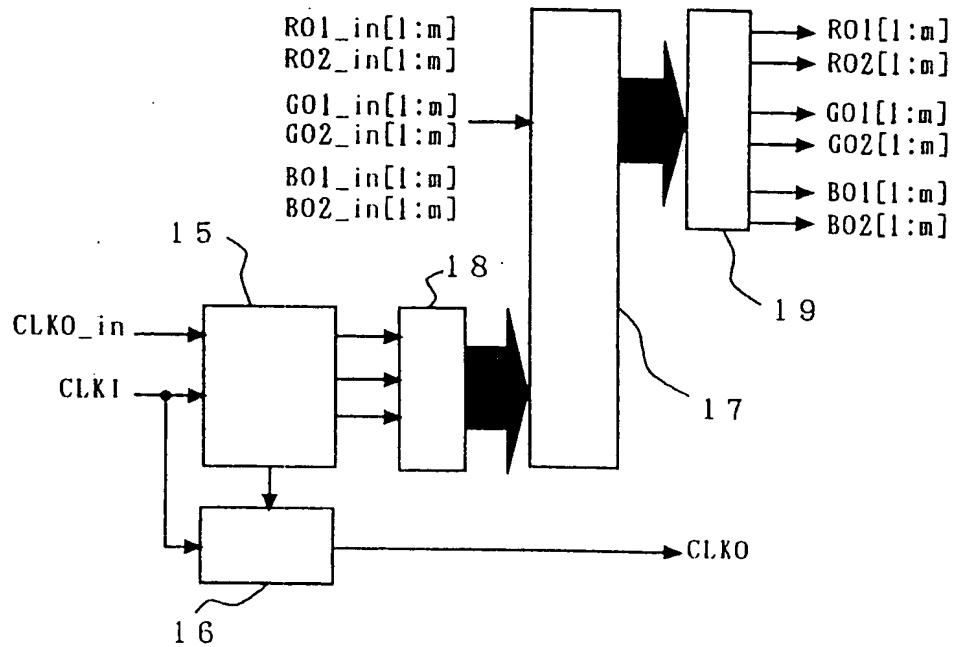


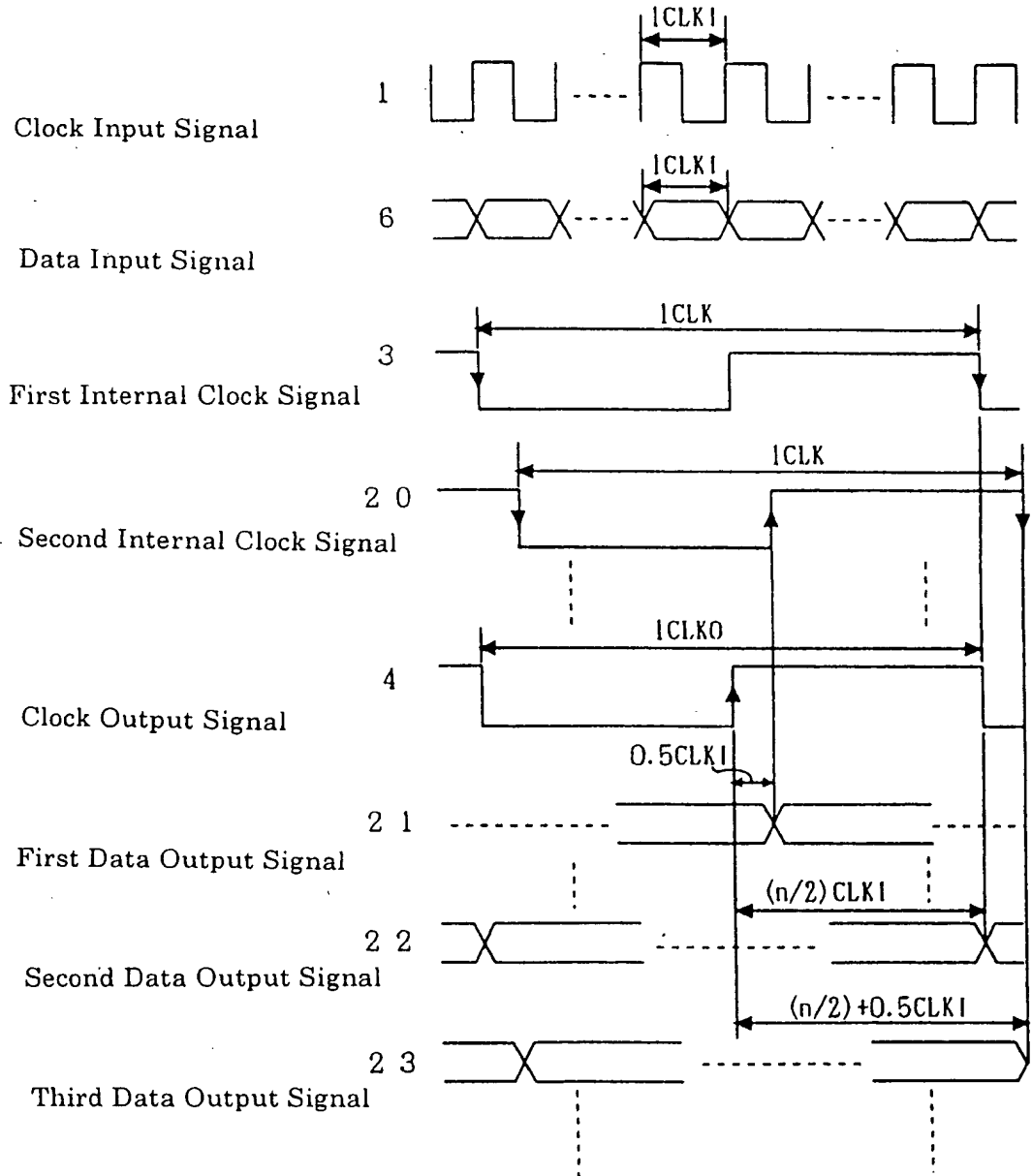
Fig 4



REPLACEMENT SHEET



Fig 5



REPLACEMENT SHEET



Fig 6

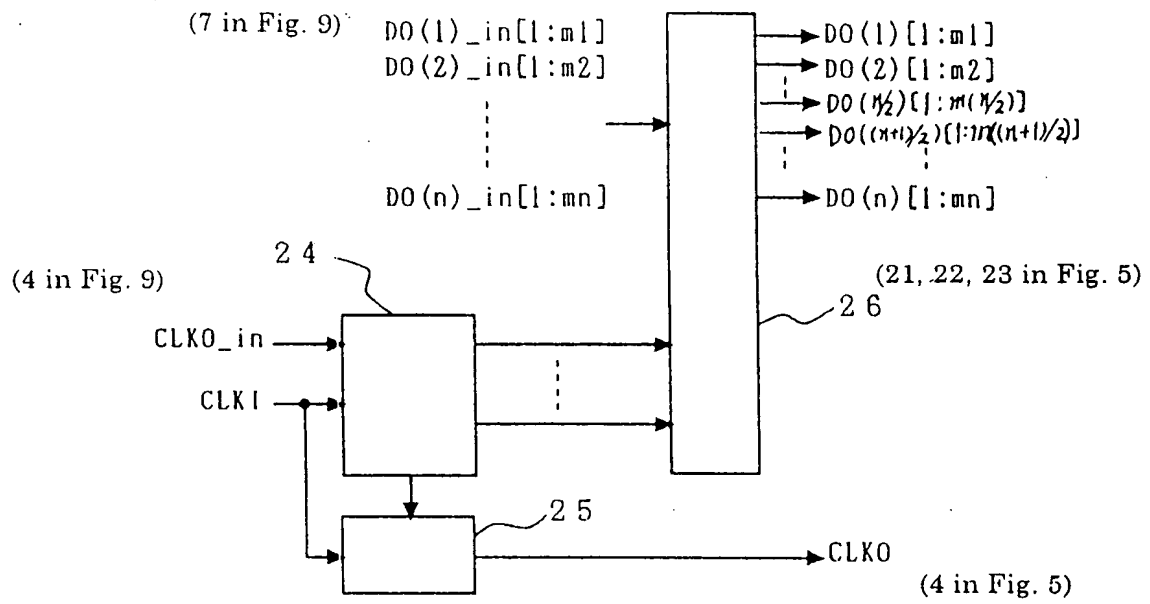


Fig 7

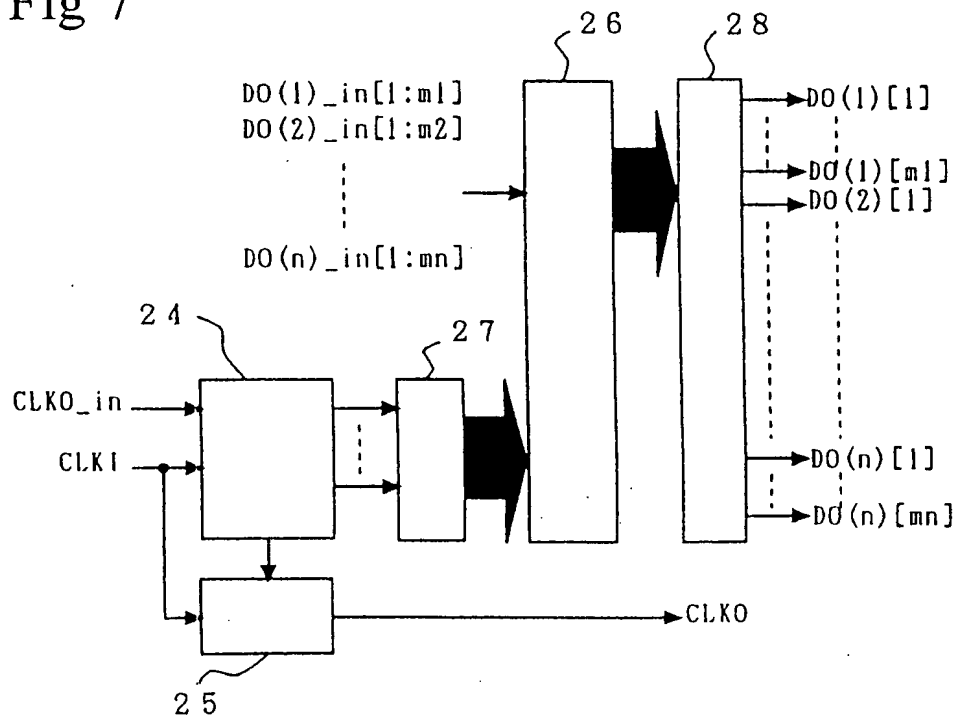




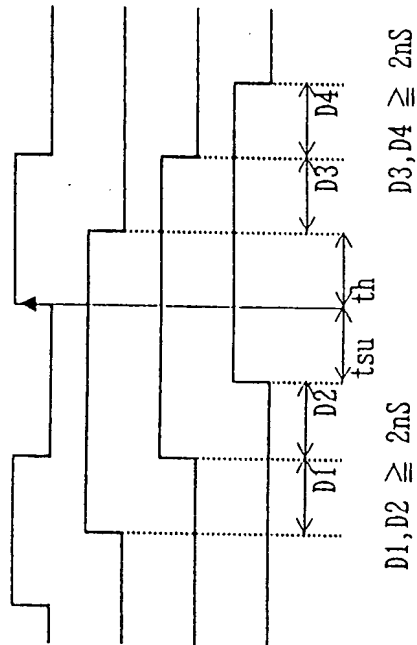
Fig 8

Data Transfer Clock

R0, R1, R2, R3, R4, R5

G0, G1, G2, G3, G4, G5

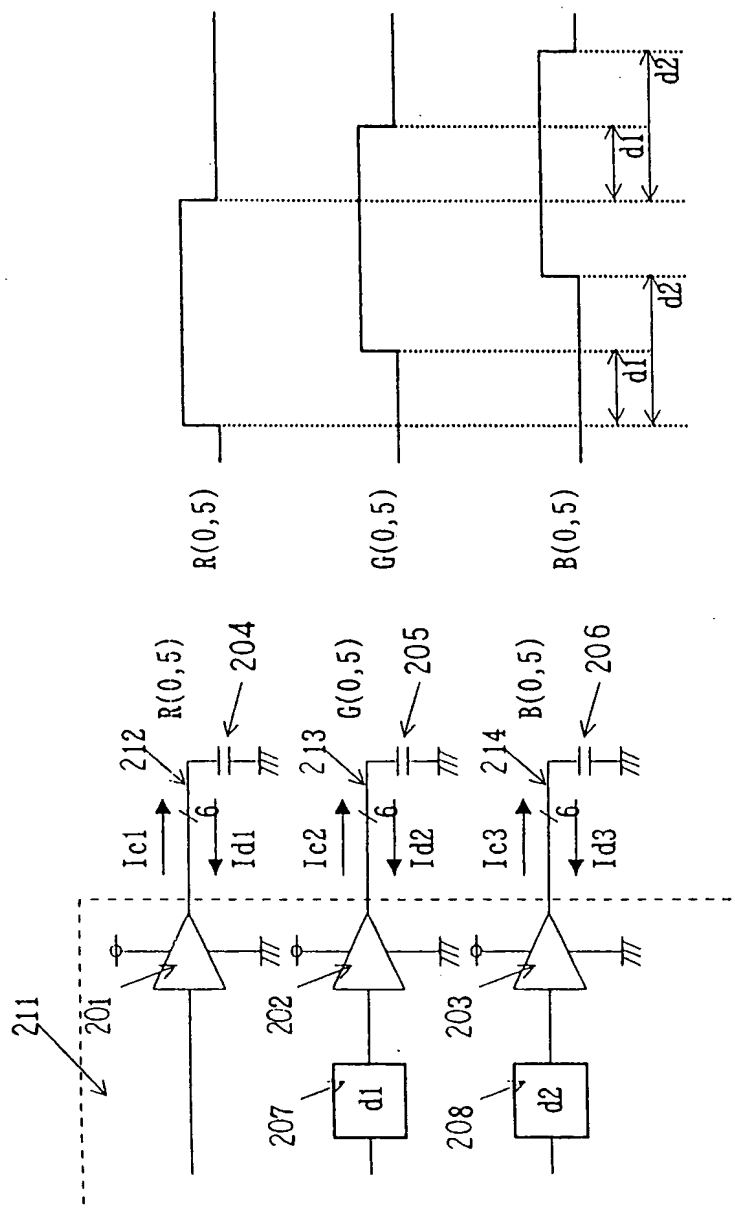
B0, B1, B2, B3, B4, B5



REPLACEMENT SHEET



Fig 9





REPLACEMENT SHEET

Fig 10

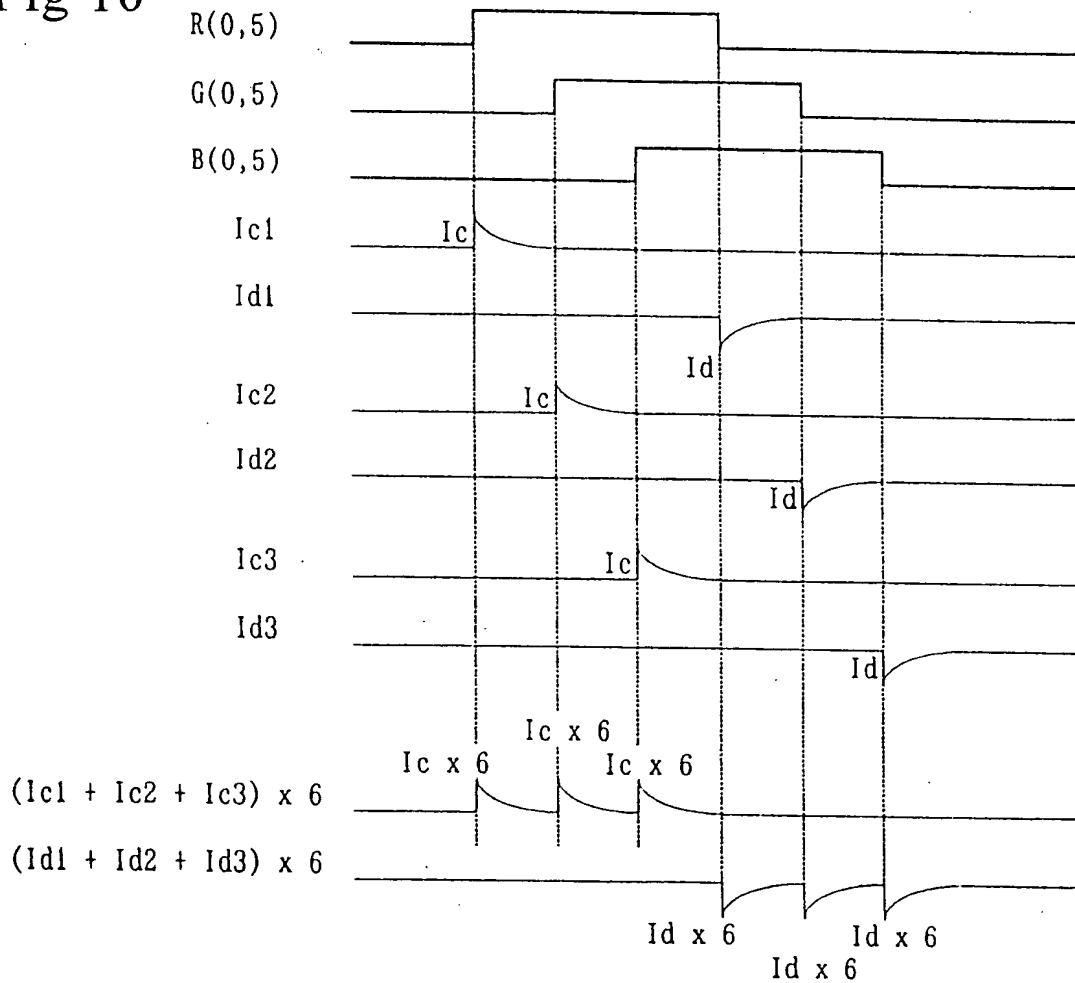


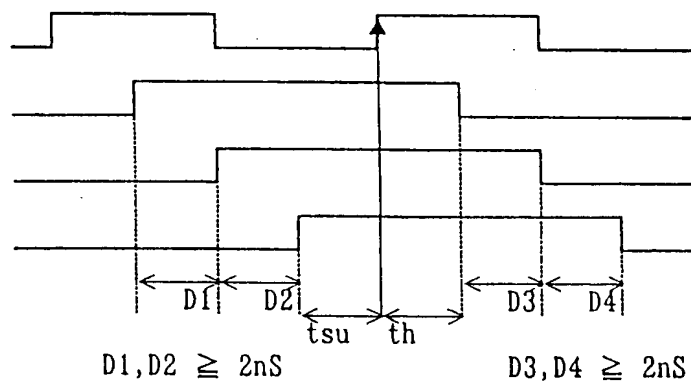
Fig 11

Data Transfer Clock

R0,R1,G0,G1,B0,B1

R2,R3,G2,G3,B2,B3

R4,R5,G4,G5,B4,B5



REPLACEMENT SHEET



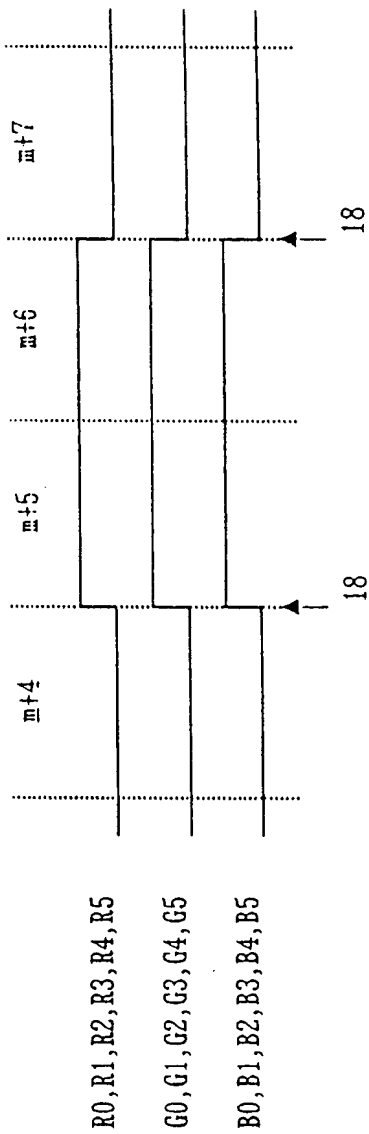
Fig 12

	m	m+1	m+2	m+3	m+4	m+5	m+6	m+7	m+8	m+9	m+10	m+11	m+12	m+13	m+14	m+15
n	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+1	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+2	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+3	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+4	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+5	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+6	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+7	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+8	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+9	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+10	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB
n+11	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB	RGB

Fig 13

	m+4			m+5			m+6			m+7		
n	R	G	B	R	G	B	R	G	B	R	G	B
n+1	R	G	B	R	G	B	R	G	B	R	G	B
n+2	R	G	B	R	G	B	R	G	B	R	G	B
n+3	R	G	B	R	G	B	R	G	B	R	G	B

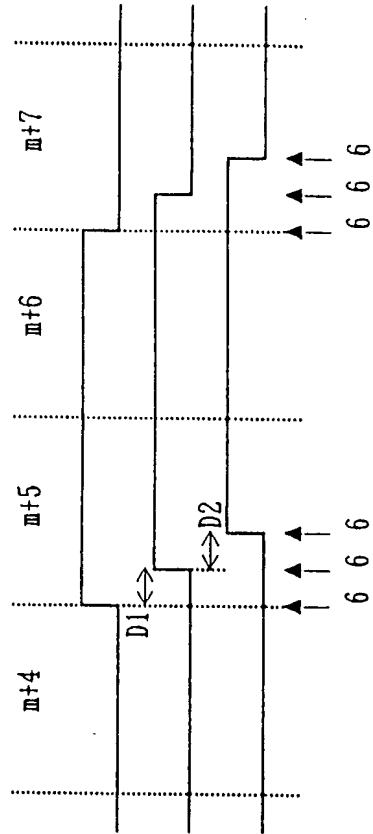
Fig 14



REPLACEMENT SHEET



Fig 15



R0, R1, R2, R3, R4, R5

G0, G1, G2, G3, G4, G5

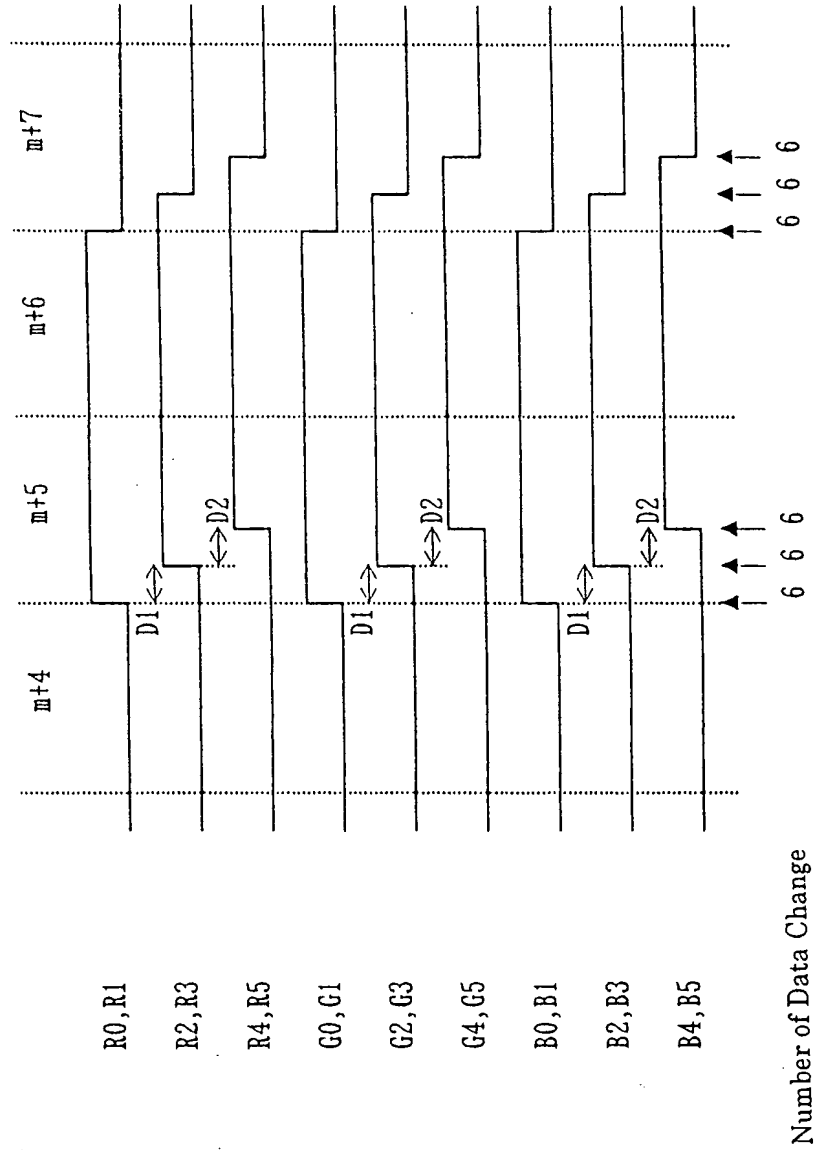
B0, B1, B2, B3, B4, B5

Number of Data Change

REPLACEMENT SHEET



Fig 16



REPLACEMENT SHEET

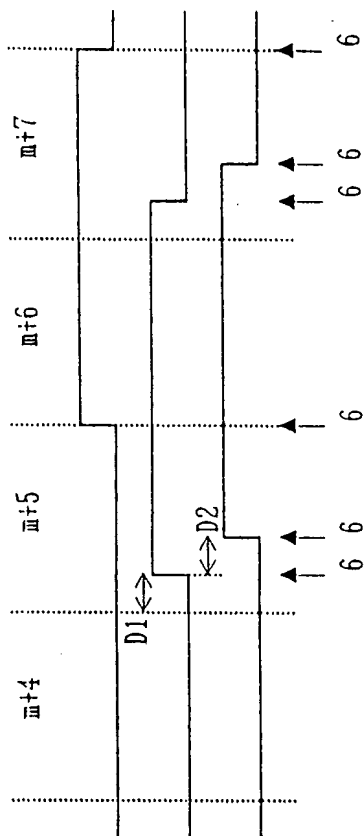


Fig 17

	m+4			m+5			m+6			m+7		
n	R	G	B	R	G	B	R	G	B	R	G	B
n+1	R	G	B	R	G	B	R	G	B	R	G	B
n+2	R	G	B	R	G	B	R	G	B	R	G	B
n+3	R	G	B	R	G	B	R	G	B	R	G	B



Fig 18



R0, R1, R2, R3, R4, R5

G0, G1, G2, G3, G4, G5

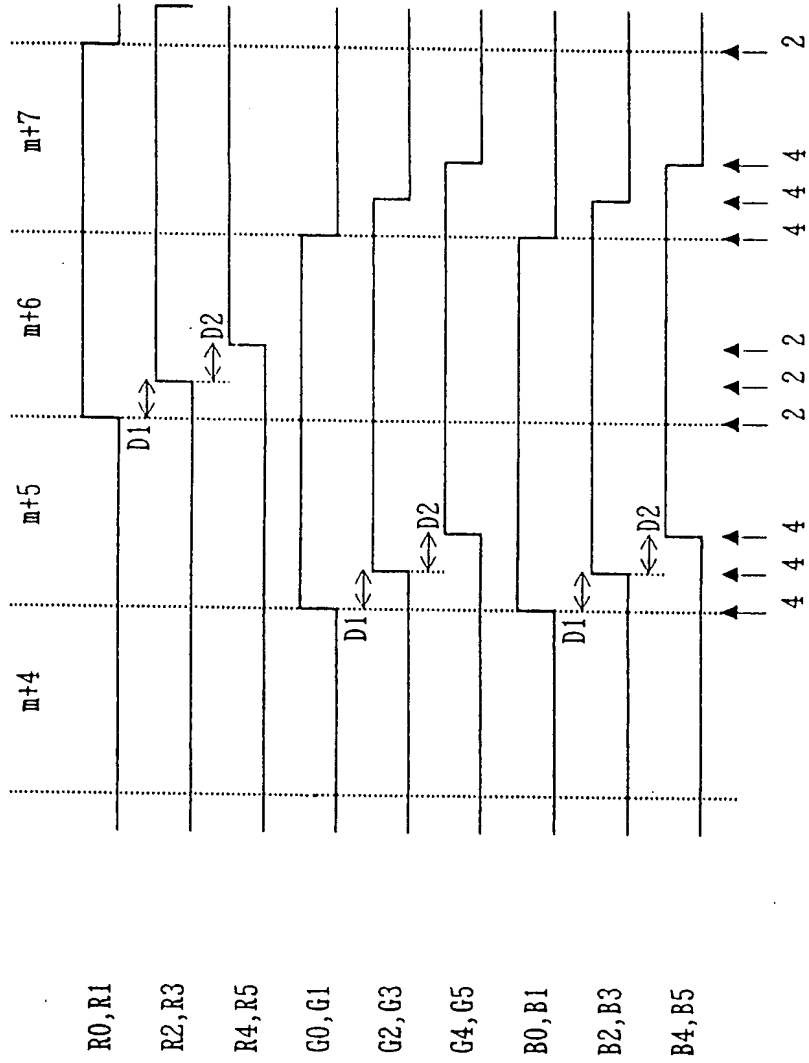
B0, B1, B2, B3, B4, B5

Number of Data Change

REPLACEMENT SHEET



Fig 19



Number of Data Change

REPLACEMENT SHEET



Fig 20

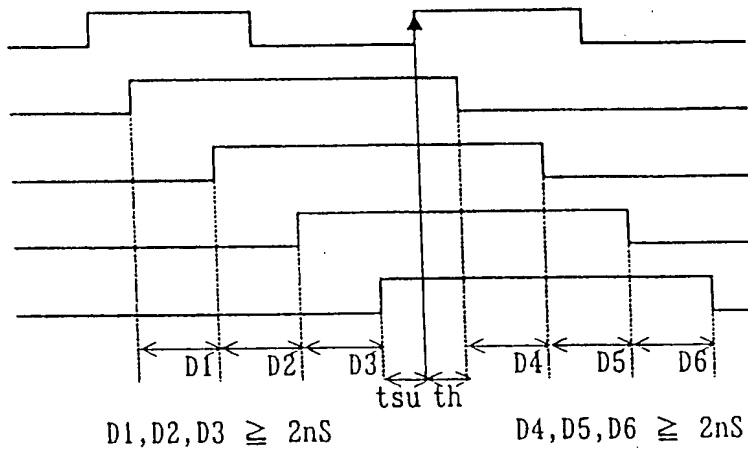
Data Transfer Clock

R0,R1,G0,G1,B0,B1

R2,R3,G2,G3,B2,B3

R4,R5,G4,G5,B4,B5

R6,R7,G6,G7,B6,B7



The diagram illustrates the internal architecture of a Source Driver IC, divided into a 'Dedicated IC Side' and a 'Source Driver IC Side' by a central wavy line representing a bus or interface.

- Dedicated IC Side (Left):**
 - Control Circuit A (317):** Receives multiple input signals labeled 315_1 , 315_2 , 315_n , 315_{n+1} , 315_{2n} , 315_{2n+1} , and 315_{3n} . It is connected to a **Comparator-Detector Circuit (316)**.
 - Comparator-Detector Circuit (316):** Outputs a signal labeled 'A' to the right side.
- Source Driver IC Side (Right):**
 - Data Processing Circuit (319):** The topmost block, which provides multiple output lines to the other components.
 - Control Circuit B (318):** Receives signals from the Data Processing Circuit and has bidirectional connections with the Data Processing Circuit.
- Inter-Side Connections:**
 - Signals from the Data Processing Circuit (319) cross the central boundary to connect with Control Circuit A (317) and the Comparator-Detector Circuit (316).
 - The output 'A' from the Comparator-Detector Circuit (316) crosses the boundary to connect with the Data Processing Circuit (319).

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Fig 22

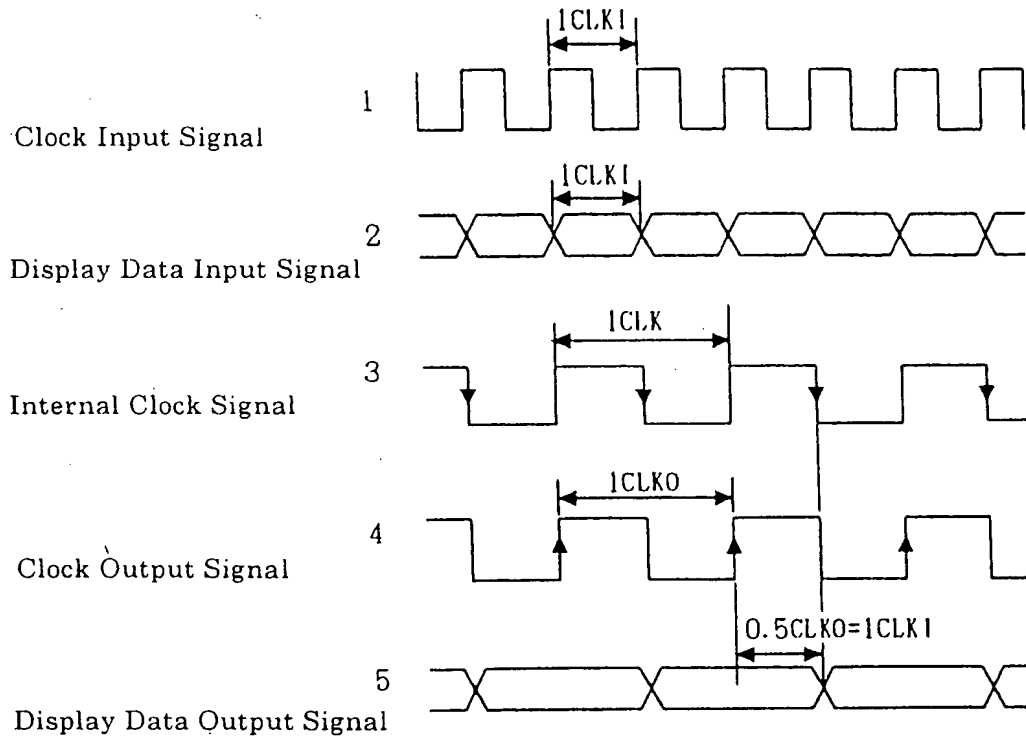
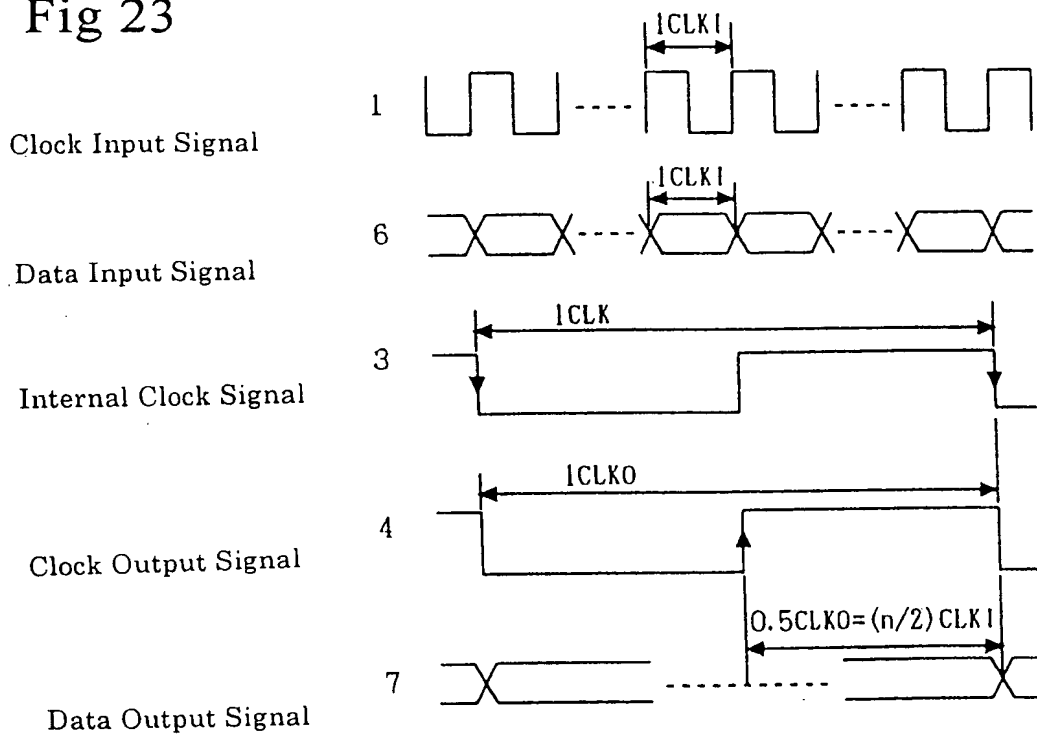


Fig 23



REPLACEMENT SHEET

Fig 24

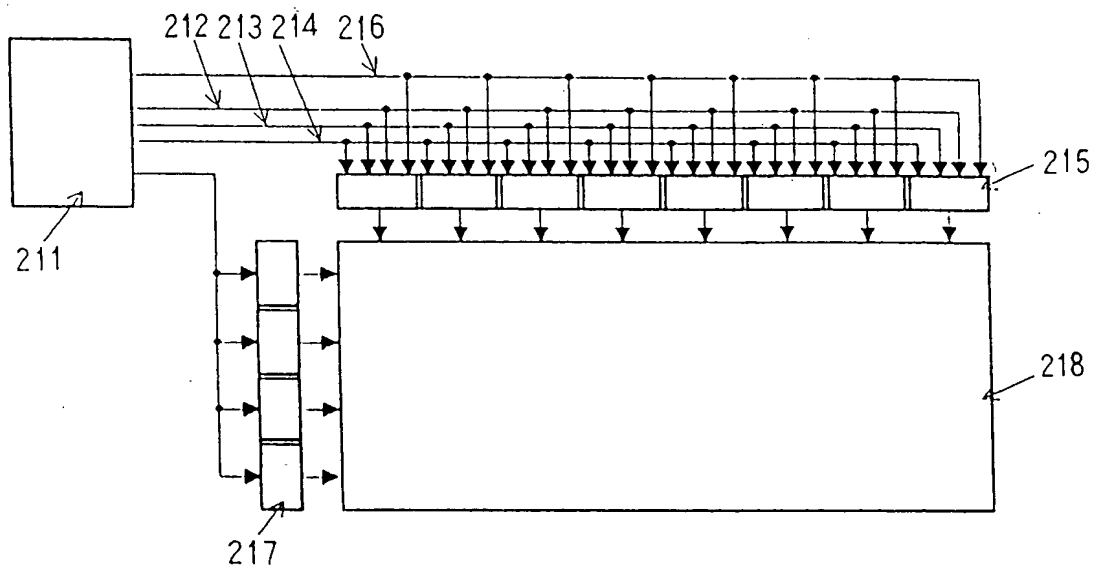
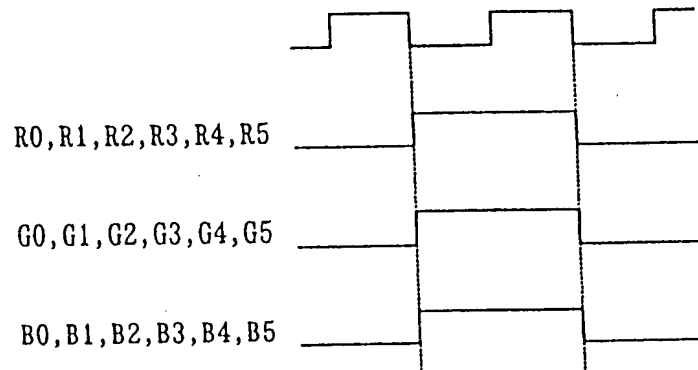


Fig 25

Data Transfer Clock



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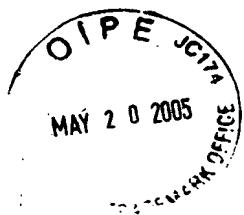
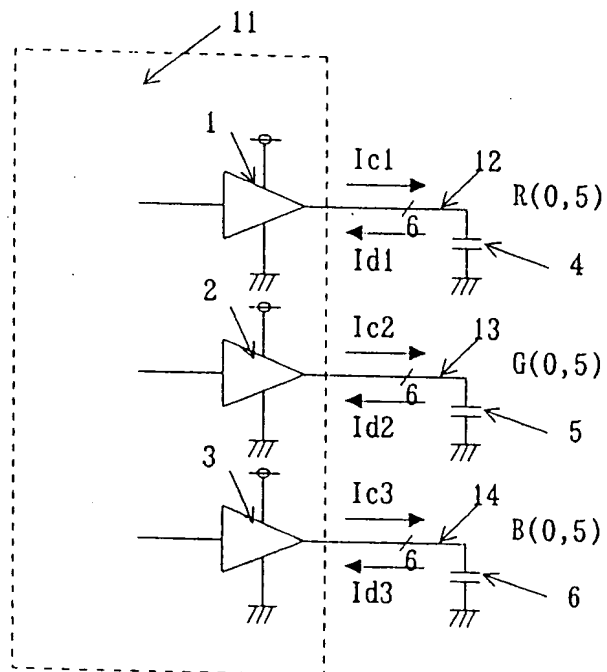


Fig 26



REPLACEMENT SHEET

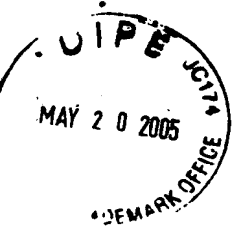


Fig 27

Data Transfer Clock

R(0,5),G(0,5),B(0,5)

Ic1

Id1

Ic2

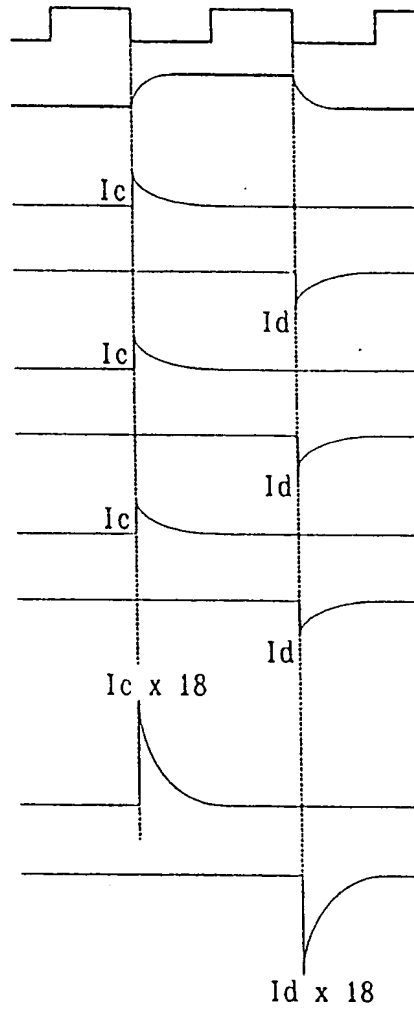
Id2

Ic3

Id3

$(Ic1 + Ic2 + Ic3) \times 6$

$(Id1 + Id2 + Id3) \times 6$



REPLACEMENT SHEET



Fig 28

